K/Ka-BAND LOW-NOISE EMBEDDED TRANSMISSION LINE (ETL) MMIC AMPLIFIERS

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ABSTRACT

The design, fabrication, and performance of producible, high-performance K-, and Ka-band pHEMT low-noise MMIC amplifiers using embedded transmission line (ETL) circuit concept with top-side grounding are reported. A state-of-the-art noise figure of 1.2 dB with 25 dB gain is achieved at 31 GHz. These amplifiers can be implemented in low-cost, ultra-compact receiver modules for emerging spaceborne phased-array communication applications.

INTRODUCTION

The Embedded Transmission Line (ETL) MMIC approach first reported in [1] utilizes matching circuits with transmission lines and lumped passive components (resistors, series/shunt capacitors, and spiral inductors) embedded in a low-K dielectric (polyimide) medium coated over the active devices. The quasi-hermetic nature of the ETL MMIC simplifies the packaging requirement for high-density microwave/millimeter-wave module integration. In this paper, highly uniform performance from a K-band low-noise amplifier design and state-of-the-art noise performance from a Ka-band MMIC design are reported.

EMBEDDED TRANSMISSION LINE (ETL) MMIC TECHNOLOGY

The Embedded Transmission Line (ETL) MMIC approach uses matching circuits with transmission lines and lumped passive components embedded in a low-K dielectric (such as polyimide) medium. Figure 1 shows the sketch of an ETL MMIC cross section with an unthinned GaAs substrate. The MMIC can be used either upright (top-side ground with the GaAs substrate down) or in inverted configuration with flipped transistors for efficient heat transfer and low common-lead inductance. This approach differs from the traditional MMIC design in that transistor sources (FET) or emitters (BJT) are individually grounded to the top-side ground plane (through plated heatsink over source or emitter interconnect bridges) to provide excellent heat transfer (in inverted configuration) and low-inductance ground connections. Other passive components such as transmission lines, resistors, and capacitors are fabricated on the

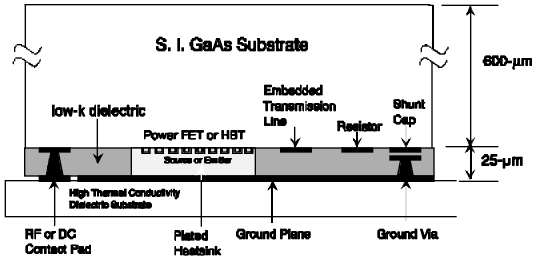

Figure 1: ETL Power MMIC with Flipped Transistor

GaAs as before; they are redesigned taking into account the new circuit configuration with mixed dielectric (i.e., low-K dielectric and GaAs substrate). Shunt components such as MIM capacitors and/or shorted transmission line stubs are readily grounded through gold plugs in the thin dielectric rather than the GaAs substrate as in the conventional MMIC approach. The thickness of the dielectric layer can be on the same order as the plated source/emitter (25 to 50 µm). For RF I/O and dc biases, connecting pads are isolated from the top-side ground plane, allowing for on-wafer testing and versatile interconnections to other module components through multilayer interconnect board. In the configuration shown in Figure 1 with unthinned substrate, no through-GaAs substrate vias (as in the conventional MMIC case) are required for the shunt components, which greatly simplify the process and reduce the costs. If desired, the substrate can be thinned to provide an extra ground plane and through-wafer vias. This allows desirable I/O pads for vertical integration with other ETL MMIC chips or multi-layer interconnect/distribution board. The I/O and bias pads can be provided either through GaAs substrate or the polyimide layer. For thickness compatibility with other module components, the ETL MMIC chips described in this paper use 4-mil (100 µm) thick GaAs with 1-mil (25 µm) thick polyimide and double-sided ground plane.

LOW-NOISE ETL MMIC DESIGN AND PERFORMANCE

AlGaAs/InGaAs on GaAs pseudomorphic high electron mobility transistor (pHEMT) with channel structure

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optimized for low-noise performance at K/Ka-band was used. The design features 0.25 µm long T-gate with etch-stop layer for recess uniformity and high yield. The MMIC design is based on 25 µm thick polyimide and 4-mil (100 µm) thick GaAs substrate. RF on-wafer noise characterization was used for both discrete devices and MMIC amplifiers. Figure 2 shows the measured noise parameters (F_{min}, R_n, and Γ_{opt}) of a 150 µm device over 18 to 26 GHz. The minimum noise figure is about 1 dB at 21 GHz. The associated gain (not shown) is about 9 dB at the same frequency. A simplified schematic circuit diagram of the four-stage K-band amplifier is shown in Figure 3. This circuit features high-impedance transmission lines, MIM dc-blocking and RF by-pass capacitors and necessary bias stabilization RC networks for both in-band and out-of-band stabilization. A series feedback source inductance is used in each stage for stability. It also provides simultaneous noise and conjugate match for the input of the first stage. For the ETL circuit design, the characteristic impedance and effective dielectric constant of embedded transmission

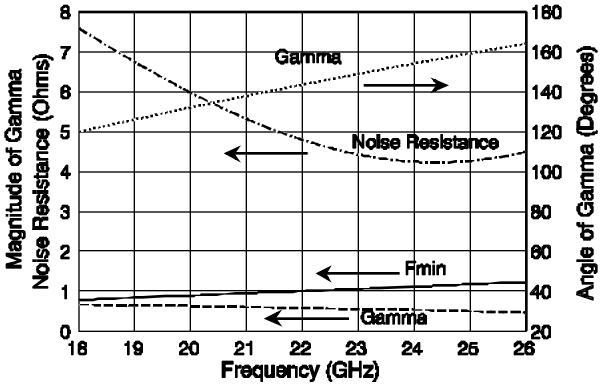

Figure 2: Noise Parameters of a 150-µm pHEMT (V_d = 3 V, V_g = +0.3 V, I_d =10 mA)

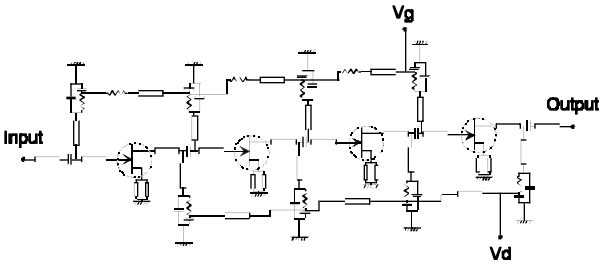

Figure 3: Four-Stage K-Band Low-Noise Amplifier Circuit

lines of various widths were obtained using a 3-D electromagnetic simulator software [1]. Figure 4 shows the K-band four-stage ETL MMIC low-noise amplifier with 150 µm gate width pHEMT in each stage. It measures 60 mils × 162 mils (no attempts were made to minimize the chip size for the first pass design). The top picture shows the top-side ground with RF I/O's and bias pads. The bottom picture shows the under-lying circuitry with the top 25-µm thick polyimide layer removed. With the exception of RF input/output pads and gate/drain pads, a solid ground plane is provided for ease of connecting to

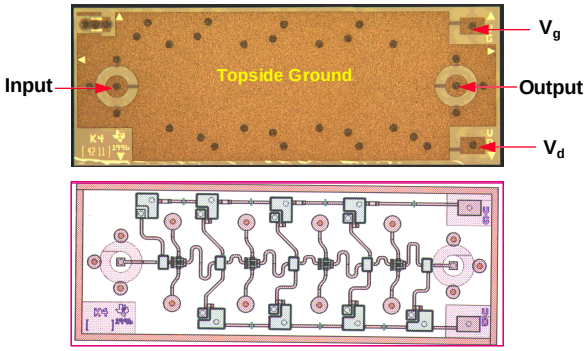

Figure 4: A Four-Stage K-Band ETL MMIC Low-Noise Amplifier

other components (i.e., solder bumps) without using bondwires with minimum mounting parasitic. Unlike most other reported bias approach with separately biased first and subsequent stages for minimum noise and high-gain, we use a single gate voltage and a single drain voltage for all stages to simplify power supply requirement for module integration. On-wafer noise characterization was used for both discrete devices and MMIC amplifiers. Only slight modification of conventional MMIC fabrication technique is required for ETL MMIC fabrication [2]. The process steps are identical up to the source interconnect level. Then, a thin layer of polyimide is applied and the first plated-metal interconnect layer is formed. Plated 25-µm height gold via "plugs" are then formed to connect the device sources and capacitors (shunt) to the ground plane. The required I/O's and bias vias are also formed at this point. A thick polyimide dielectric is then spin coated and cured to a thickness of 25 µm. Planarization and dielectric thickness control is achieved through mechanical lapping of the polyimide.

Figure 5 shows the gain/noise figure performance of a typical chip. Over most of the 18 to 26 GHz frequency band, the noise figure remains below 2 dB with the lowest noise figure of 1.3 dB at 20 and 22 GHz (the amplifier design was optimized for 20-22 GHz operation). The gain remains above 33 dB over the same band. Figures 6, 7, and 8 show, respectively, the 20 GHz noise figures, gains, and drain currents of 66 four-stage amplifier chips from the same wafer. The use of etch-stop layer for the channel recess has resulted in a remarkable uniformity across the wafer. The average noise figure is about 1.5 dB with the best noise figure of 1.2 dB. The average gain is 35 dB. It

should be noted that all amplifiers were biased at a drain voltage of 3 V and a gate voltage of +0.3 V.

Figure 9 shows a three-stage Ka-band ETL MMIC low-noise amplifier with the top polyimide layer (~ 25 µm thick) removed. The chip measures 60 × 148 mils. Like the K-band design, no attempts were made in this first pass design to minimize the chip size. Obviously, up to 30-40% reduction in chip size is possible for low cost production. Low-noise 0.25 µm long T-gate pHEMT with 100 µm gatewidth is used in each stage. The circuit topology is similar to that of the K-band amplifier shown in Figure 3. Figure 10 shows the gain and noise figure performance. A state-of-the-art noise figure of 1.2 dB with 25 dB gain is achieved at 31 GHz. The noise figure is less than 2 dB between 30 and 32 GHz. Similar to that of the four-stage K-band amplifier (Figure 4), on-chip gate and drain bias networks are used for single drain and single gate power supply operations. Our ETL MMIC noise figure results compare favorably (1 dB noise figure at 32 GHz) with the reported conventional Ka-band MMIC amplifier results using 0.15 µm gate length pHEMTs [3]. Our noise figure is lower than that reported in Reference [4] for a Ka-band MMIC LNA using 0.2 µm gate length pHEMTs.

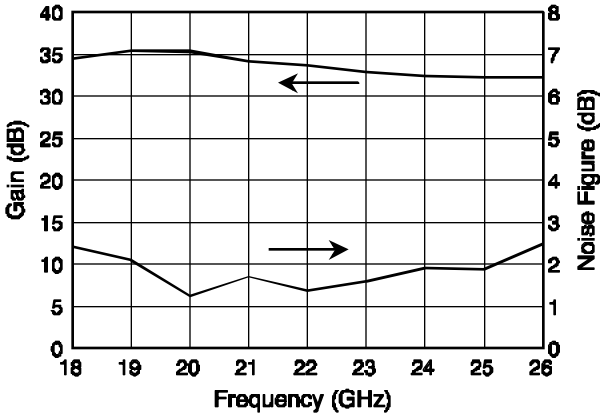

Figure 5: Performance of Four-Stage ETL MMIC Low-Noise Amplifier

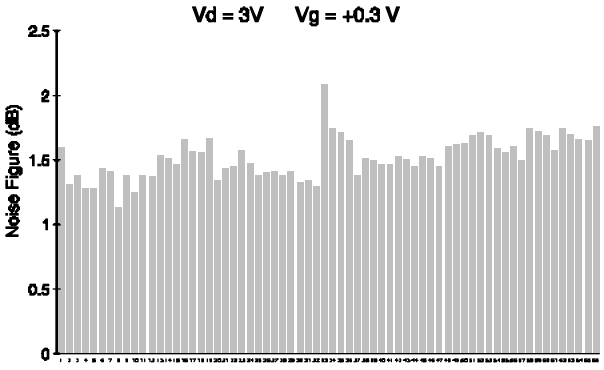

Figure 6: Noise Figure Distribution of 66 ETL K-Band LNA Chips at 20 GHz

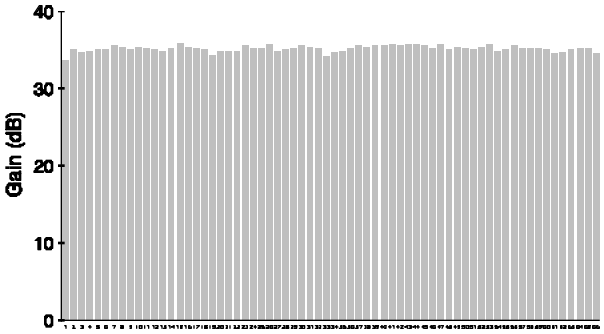

Figure 7: Gain Distribution of 66 K-Band LNA Chips

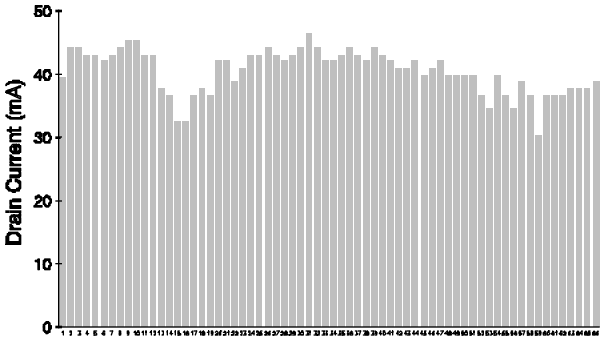

Figure 8: Drain Current Distribution of 66 K-Band LNA Chips

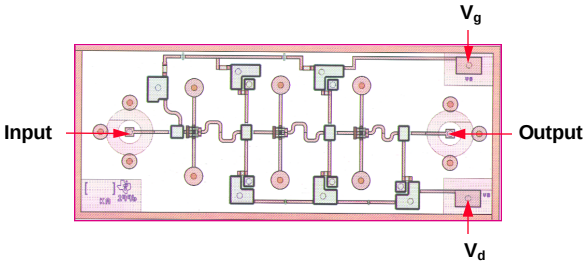

Figure 9: Three-Stage Ka-Band ETL MMIC Low-Noise Amplifier (60 × 148 mils)

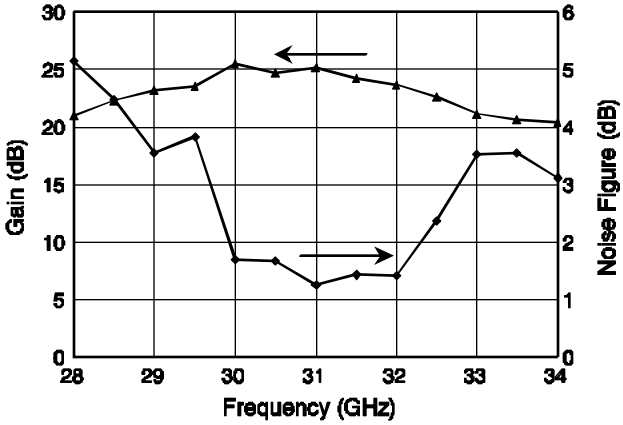

Figure 10: Performance of a Three-Stage Ka-Band ETL MMIC Low-Noise Amplifier (V_d = 3 V, V_g = +0.41 V, I_d = 35.6 mA)

CONCLUSIONS

The K/Ka-band low-noise ETL MMIC amplifiers reported in this paper can be used in low-cost, ultra-compact receiver modules for emerging spaceborne phased-array communication applications. The chip-scale packaging nature of the ETL MMIC with I/O's and bias pads suitable for flip-chip mounting using either solder bumps or Z-axis adhesives can simplify or even eliminate packaging requirements for low-cost applications.

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